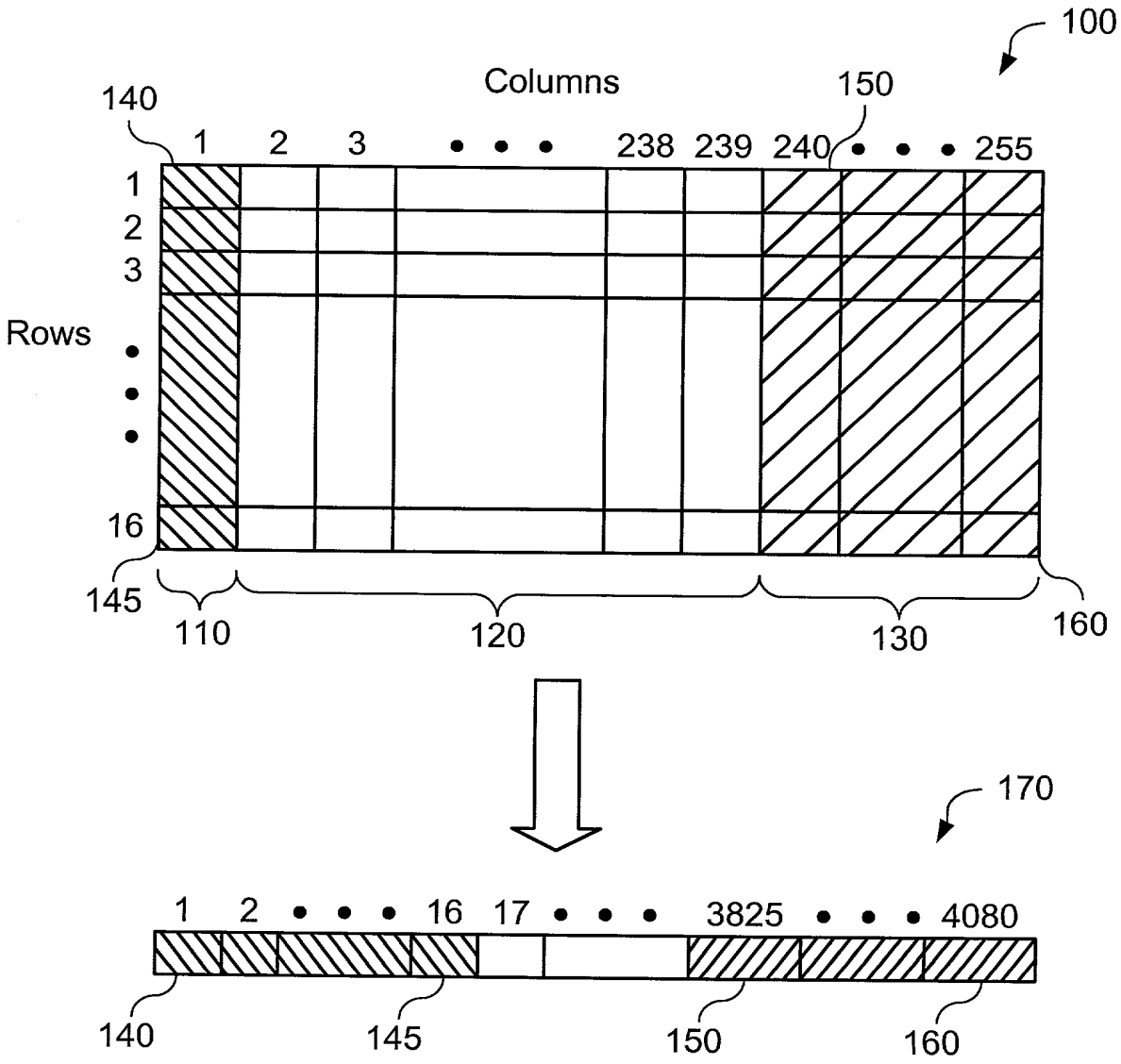


FIG. 1 (Prior Art)

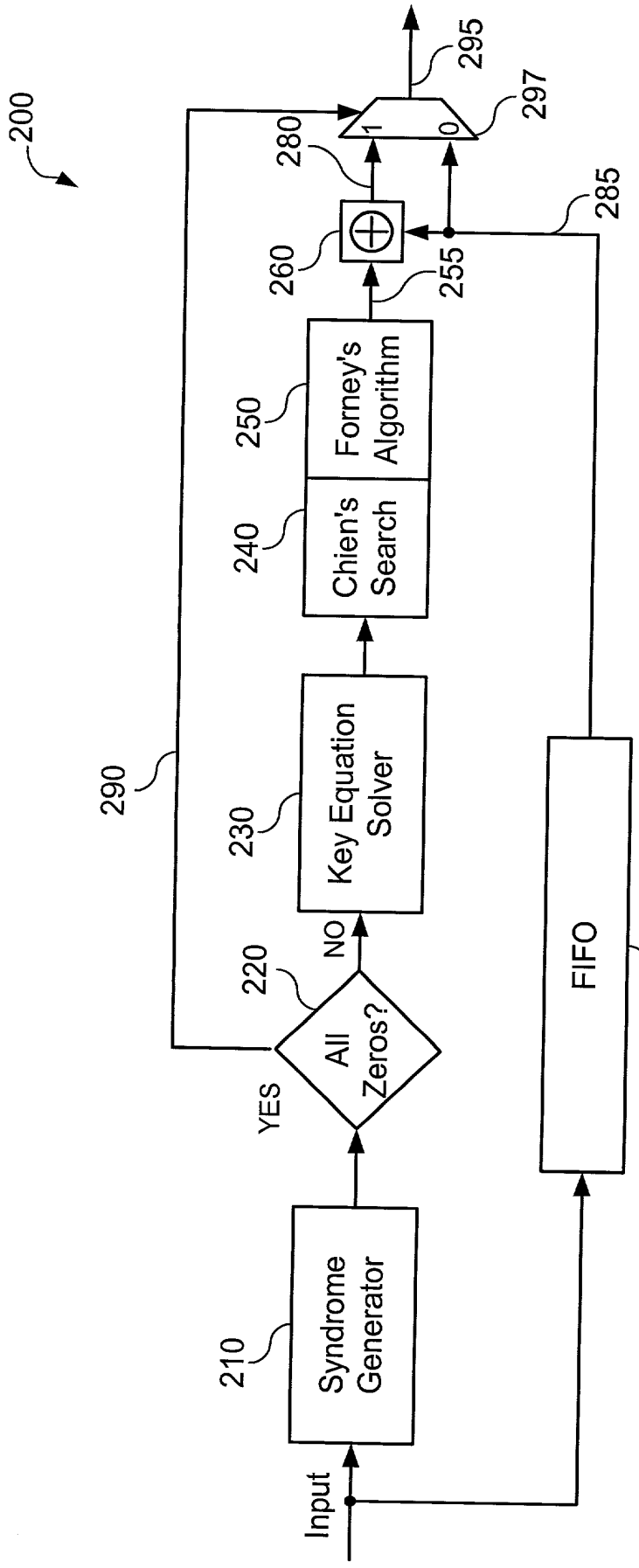


FIG. 2 (Prior Art)

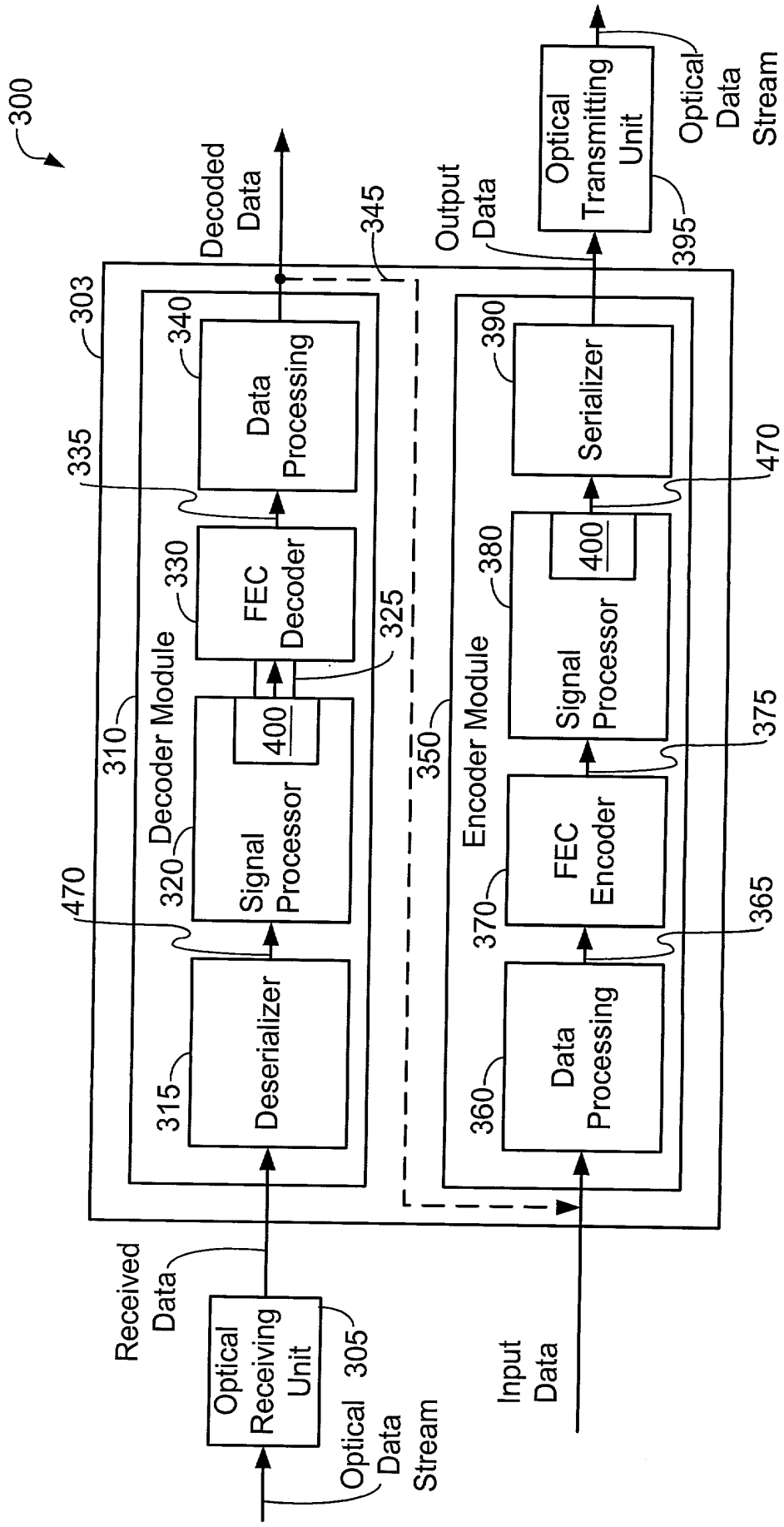

300
Optical Receiving Unit
305
Optical Data Stream
Received Data
Deserializer
315
Signal Processor
320
400
470
Decoder Module
310
FEC Decoder
330
325
Data Processing
340
335
303
Decoded Data
345
Input Data
Data Processing
360
FEC Encoder
370
365
Signal Processor
380
400
375
Encoder Module
350
Serializer
390
470
Output Data
Optical Transmitting Unit
395
Optical Data Stream

FIG. 3

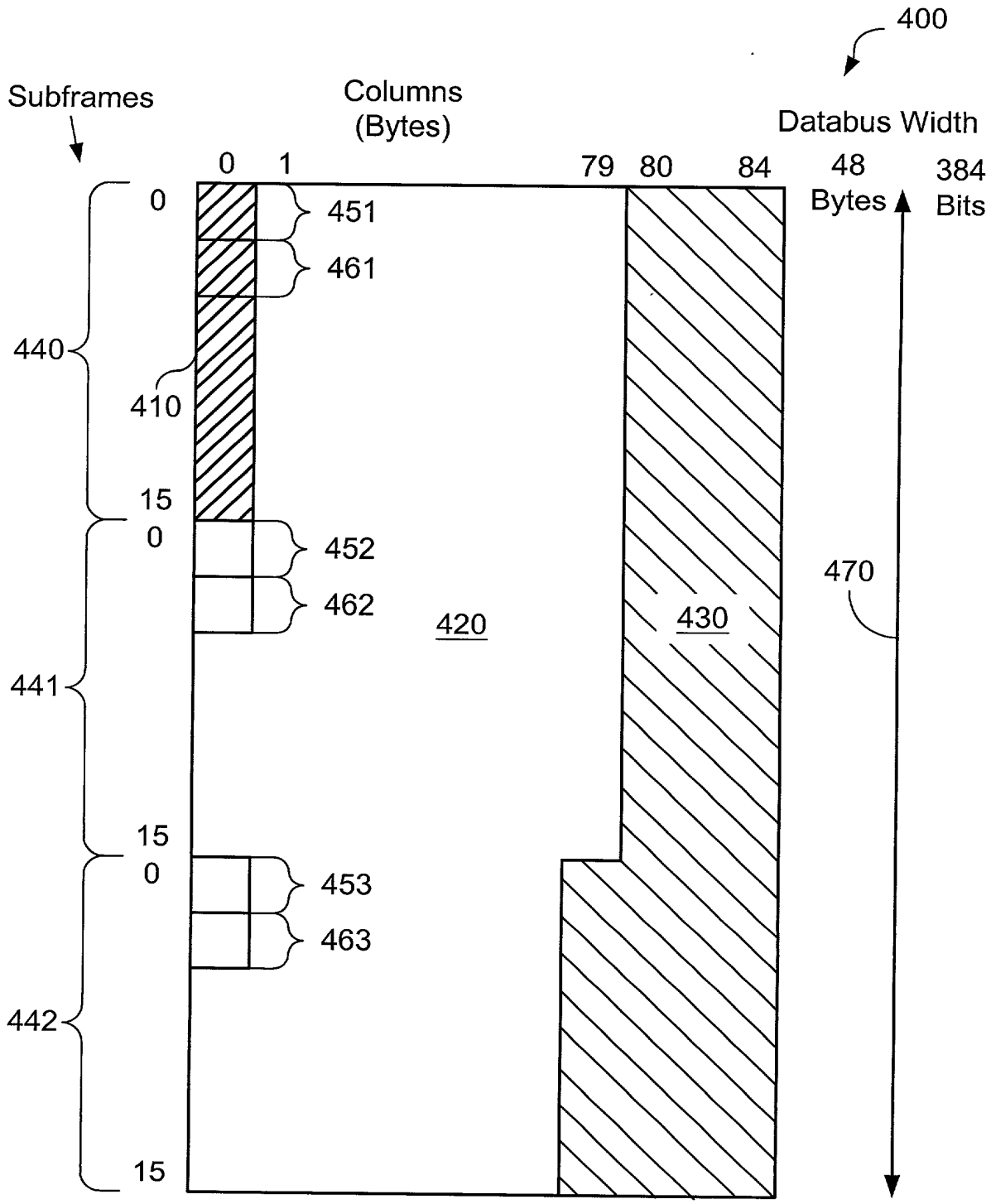

400
Subframes
Columns
(Bytes)
Databus Width
0
1
79
80
84
48
Bytes
384
Bits
0
451
461
440
410
15
0
452
462
441
420
430
470
15
0
453
463
442
15

FIG. 4

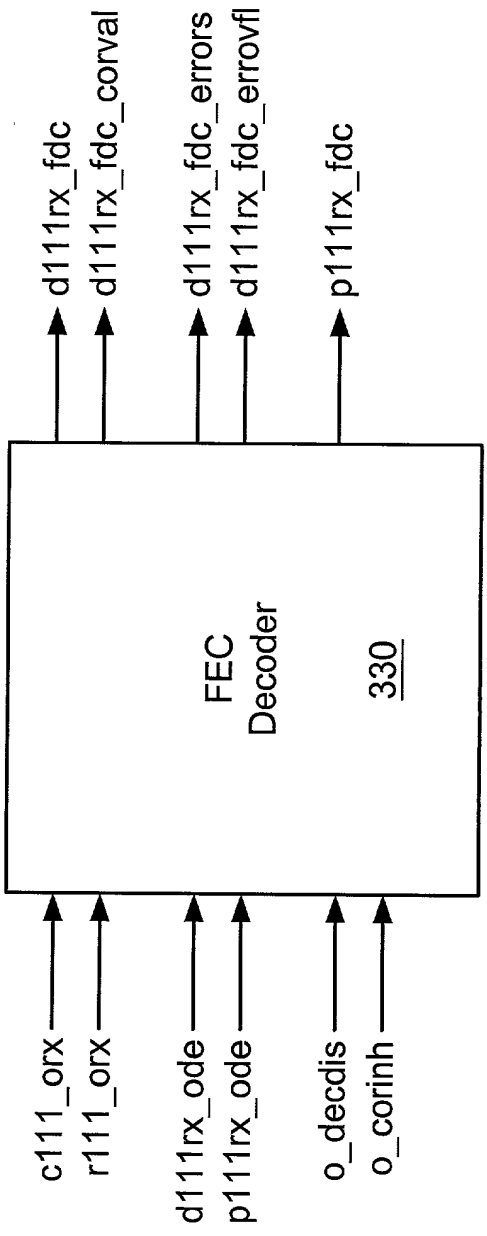

d111rx_fdc
d111rx_fdc_corval
d111rx_fdc_errors
d111rx_fdc_errovfl
p111rx_fdc
FEC
Decoder
330
c111_orx
r111_orx
d111rx_ode
p111rx_ode
o_decdis
o_corinh

FIG. 5

Name	Direction	Width	Description
c111_orx	IN	std_ulogic	System clock, 111 MHz
r111_orx	IN	std_ulogic	Signal for synchronous reset of decoder
d111rx_ode	IN	(383 down to 0)	Input encoded data
p111rx_ode	IN	std_ulogic	Start of input FEC block pulse
o_decdis	IN	std_ulogic	Decoder function enable ('1' = decoder is disabled)
o_corinh	IN	std_ulogic	Error correction enable ('1' = error correction inhibited)
d111rx_fdc	BUFFER	(383 down to 0)	Output decoded data
d111rx_fdc_corval	BUFFER	(383 down to 0)	Output correction values: This signal indicates the bit position in the data stream d111rx_fdc where a bit has been corrected (values: '0' = no correction; '1' = correction)
p111rx_fdc	BUFFER	std_ulogic	Pulse indicating the start of an output FEC block
d111rx_fdc_errors	BUFFER	(10 down to 0)	Number of corrected bit errors within one frame
d111rx_fdc_errovfl	BUFFER	(4 down to 0)	Number of uncorrectable blocks within one frame

FIG. 6

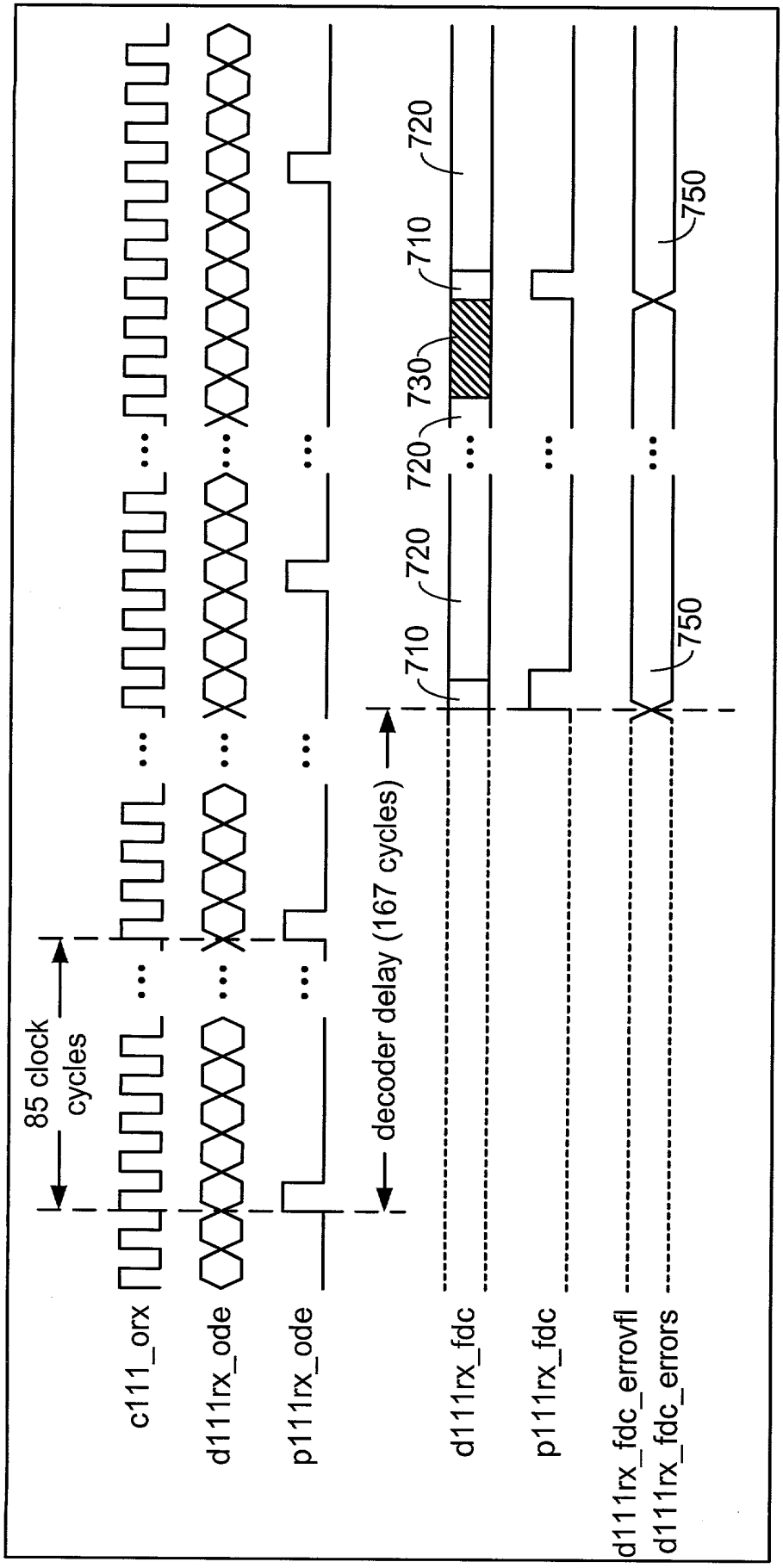

85 clock cycles
c111_orx
d111rx_ode
p111rx_ode
decoder delay (167 cycles)
d111rx_fdc
p111rx_fdc
d111rx_fdc_errovfl
d111rx_fdc_errors
710
720
730
750

FIG. 7

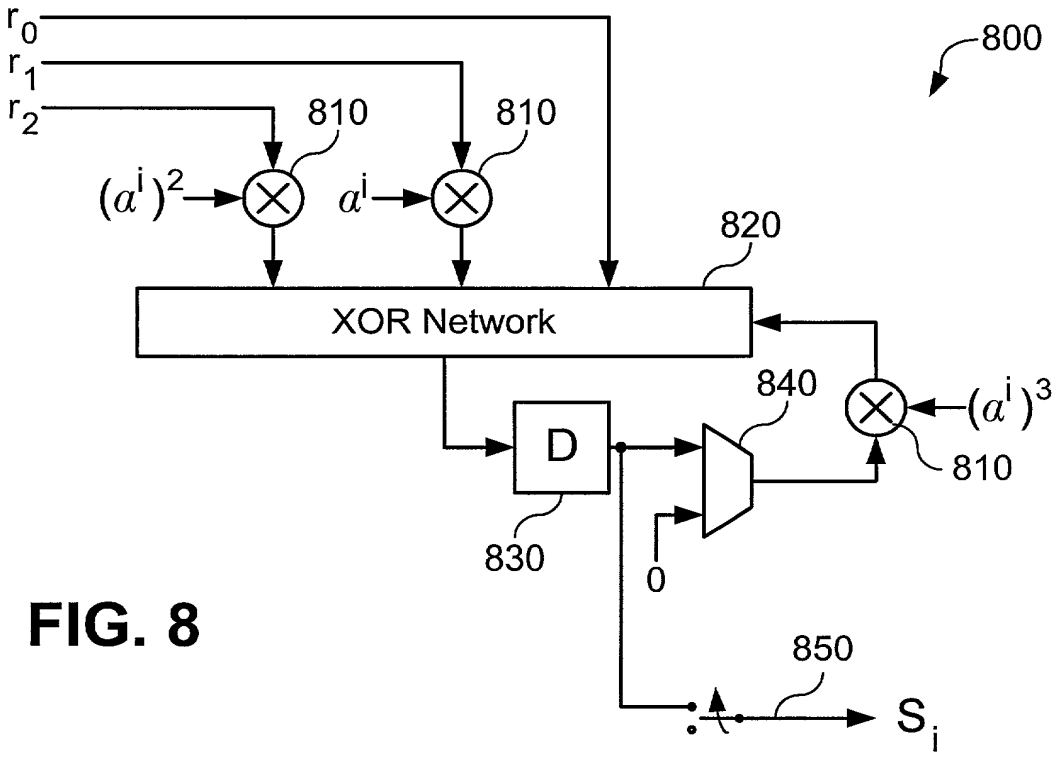

r0
r1
r2
800
810
810
$(a^i)^2$
a^i
820
XOR Network
840
$(a^i)^3$
D
810
830
0
850
S_i

FIG. 8

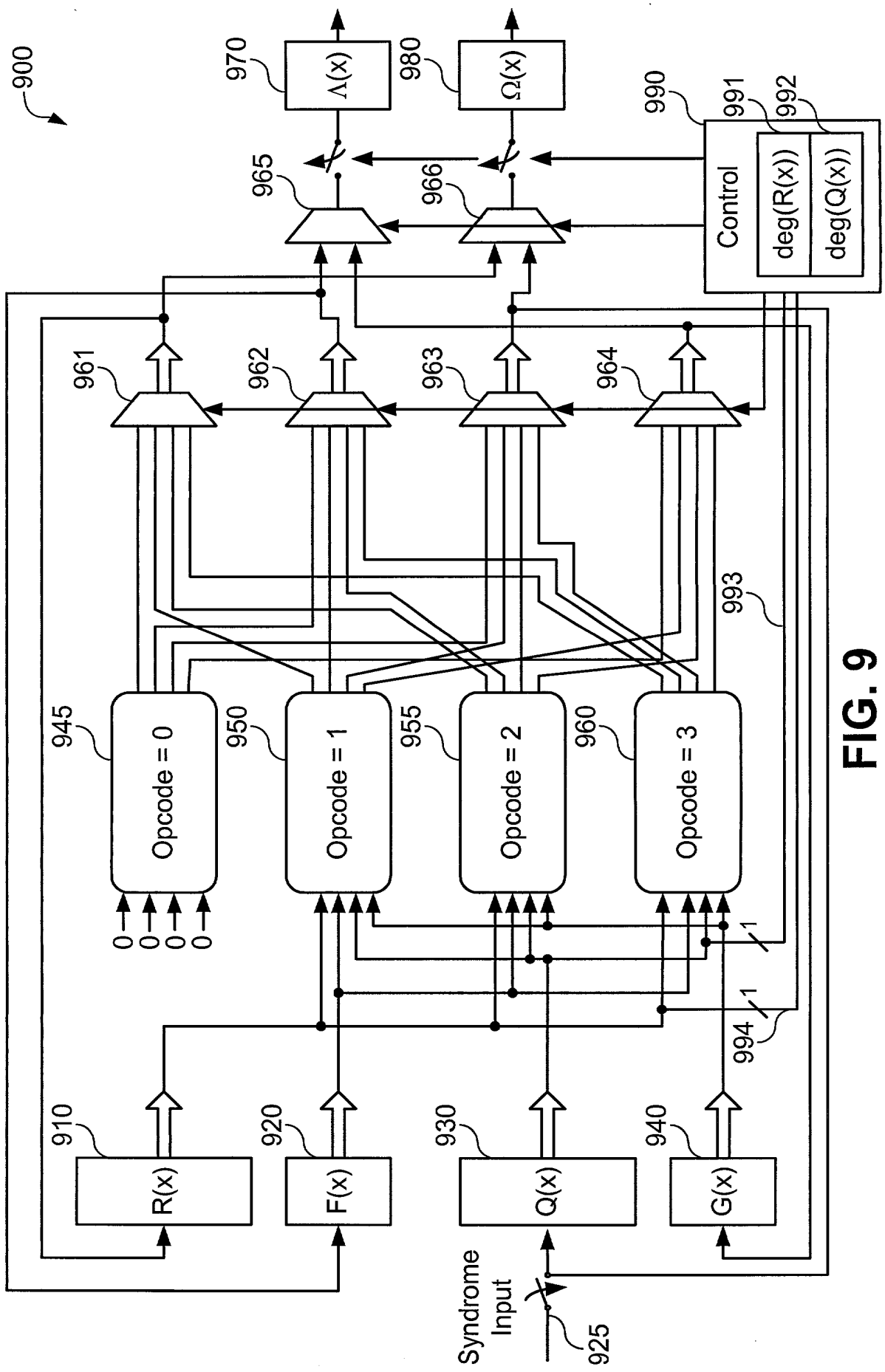

900
970
Λ(x)
980
Ω(x)
990
991
992
Control
deg(R(x))
deg(Q(x))
965
966
961
962
963
964
993
945
Opcode = 0
950
Opcode = 1
955
Opcode = 2
960
Opcode = 3
0
0
0
0
1
1
994
910
R(x)
920
F(x)
930
Q(x)
940
G(x)
Syndrome
Input
925

FIG. 9

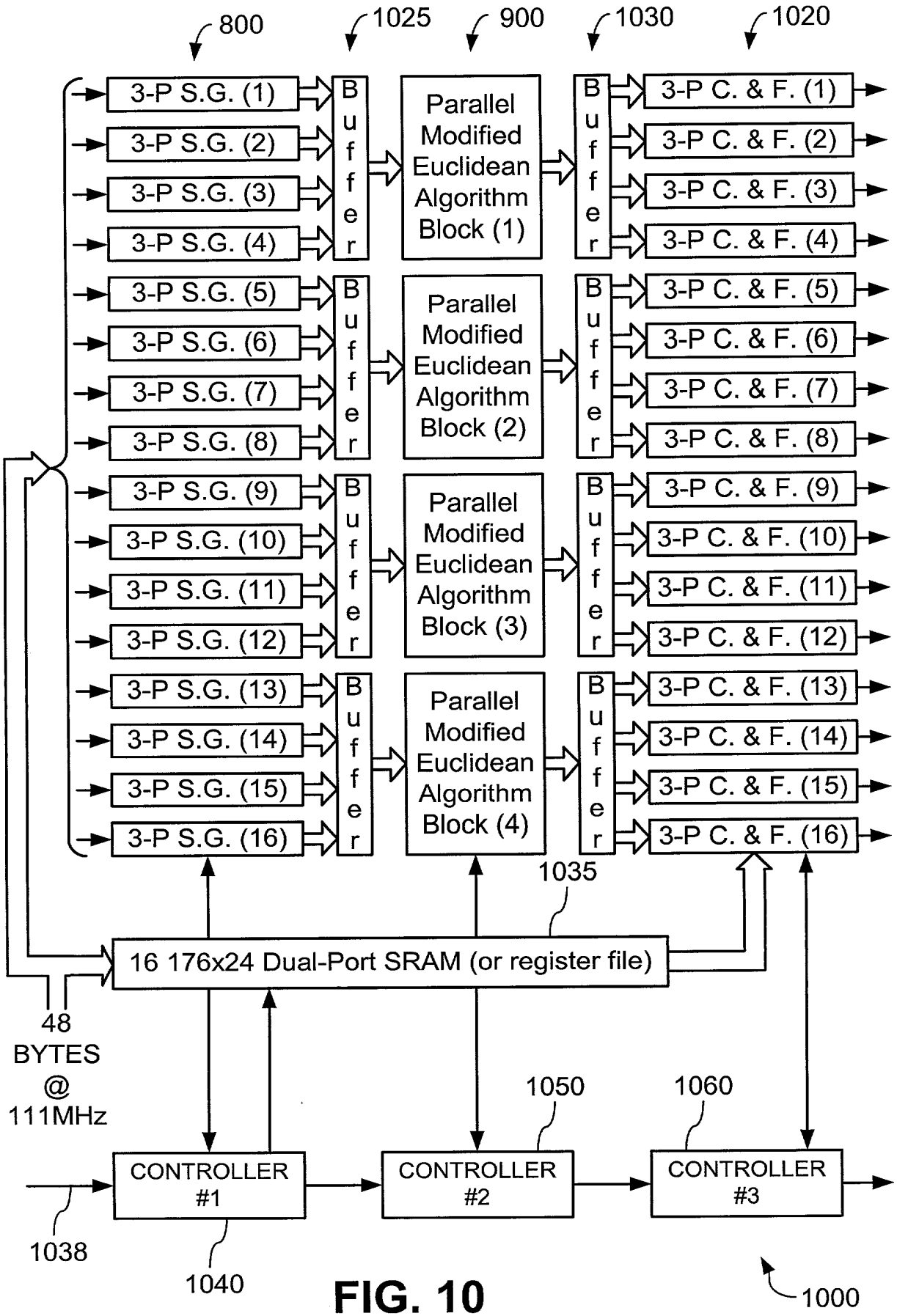

800
1025
900
1030
1020
3-P S.G. (1)
3-P S.G. (2)
3-P S.G. (3)
3-P S.G. (4)
3-P S.G. (5)
3-P S.G. (6)
3-P S.G. (7)
3-P S.G. (8)
3-P S.G. (9)
3-P S.G. (10)
3-P S.G. (11)
3-P S.G. (12)
3-P S.G. (13)
3-P S.G. (14)
3-P S.G. (15)
3-P S.G. (16)
Buffer
Parallel Modified Euclidean Algorithm Block (1)
Parallel Modified Euclidean Algorithm Block (2)
Parallel Modified Euclidean Algorithm Block (3)
Parallel Modified Euclidean Algorithm Block (4)
3-P C. & F. (1)
3-P C. & F. (2)
3-P C. & F. (3)
3-P C. & F. (4)
3-P C. & F. (5)
3-P C. & F. (6)
3-P C. & F. (7)
3-P C. & F. (8)
3-P C. & F. (9)
3-P C. & F. (10)
3-P C. & F. (11)
3-P C. & F. (12)
3-P C. & F. (13)
3-P C. & F. (14)
3-P C. & F. (15)
3-P C. & F. (16)
1035
16 176x24 Dual-Port SRAM (or register file)
48 BYTES @ 111MHz
1050
1060
CONTROLLER #1
CONTROLLER #2
CONTROLLER #3
1038
1040
1000

FIG. 10

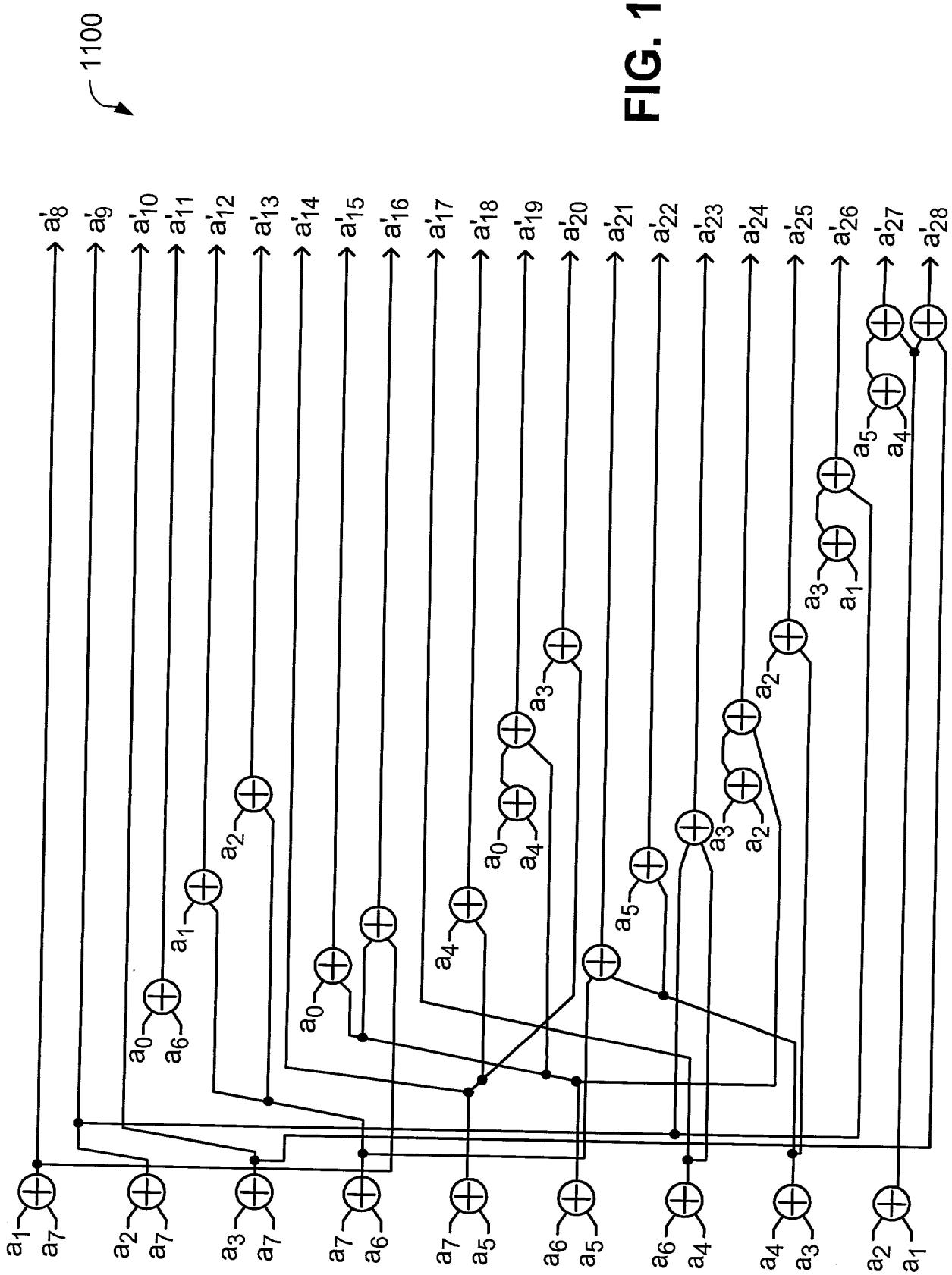

1100
a'8
a'9
a'10
a'11
a'12
a'13
a'14
a'15
a'16
a'17
a'18
a'19
a'20
a'21
a'22
a'23
a'24
a'25
a'26
a'27
a'28
a1
a7
a2
a7
a3
a7
a7
a6
a7
a5
a6
a5
a6
a4
a4
a3
a2
a1
a0
a6
a0
a1
a2
a0
a4
a4
a0
a3
a5
a3
a2
a2
a3
a1
a5
a4

FIG. 11

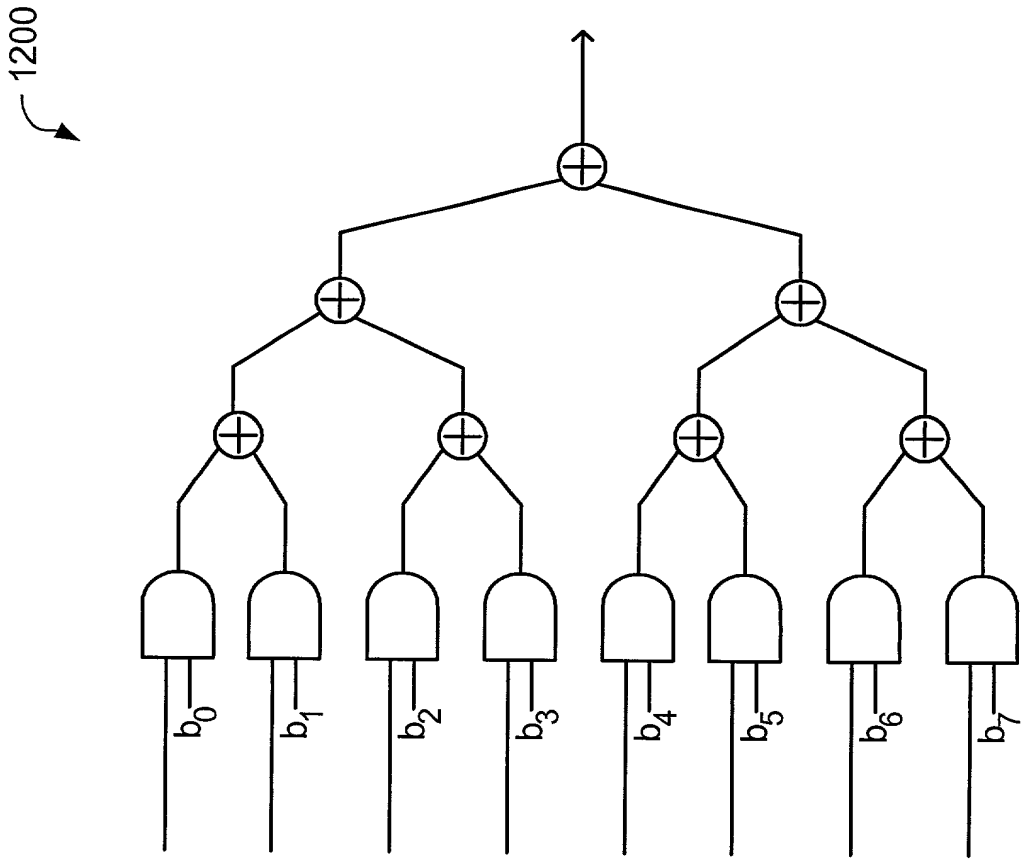


FIG. 12

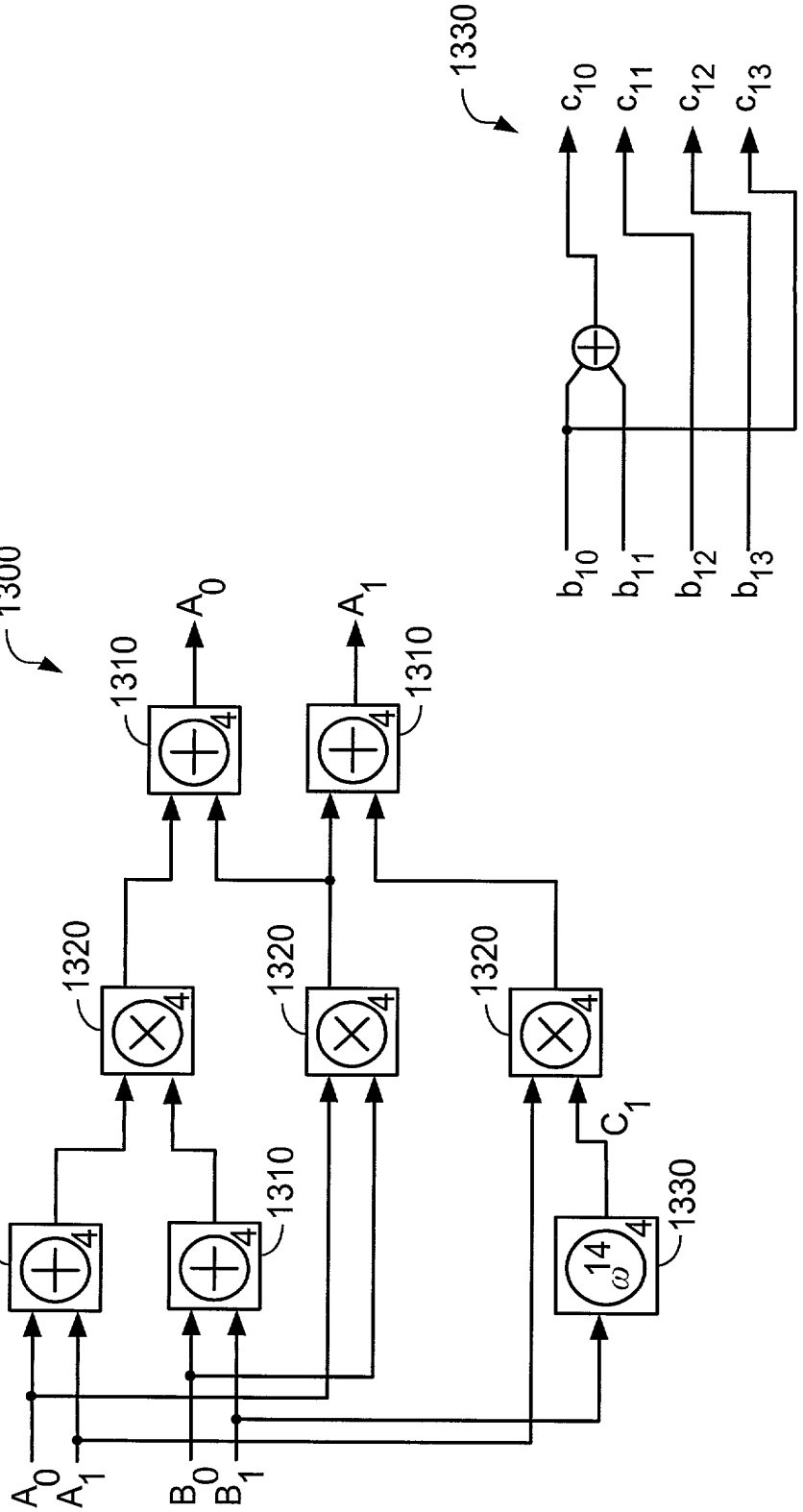


FIG. 13A

FIG. 13B

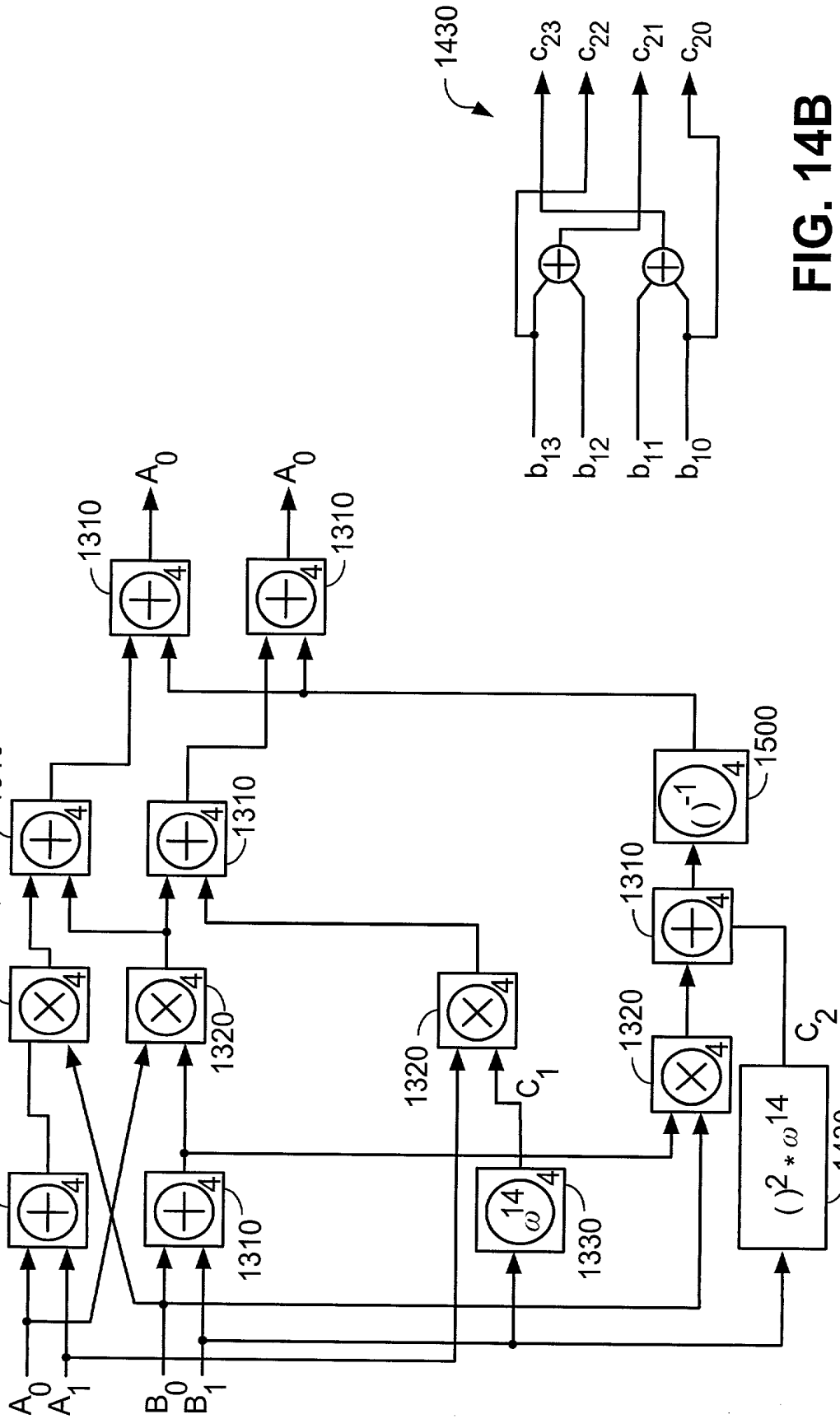


FIG. 14A

FIG. 14B

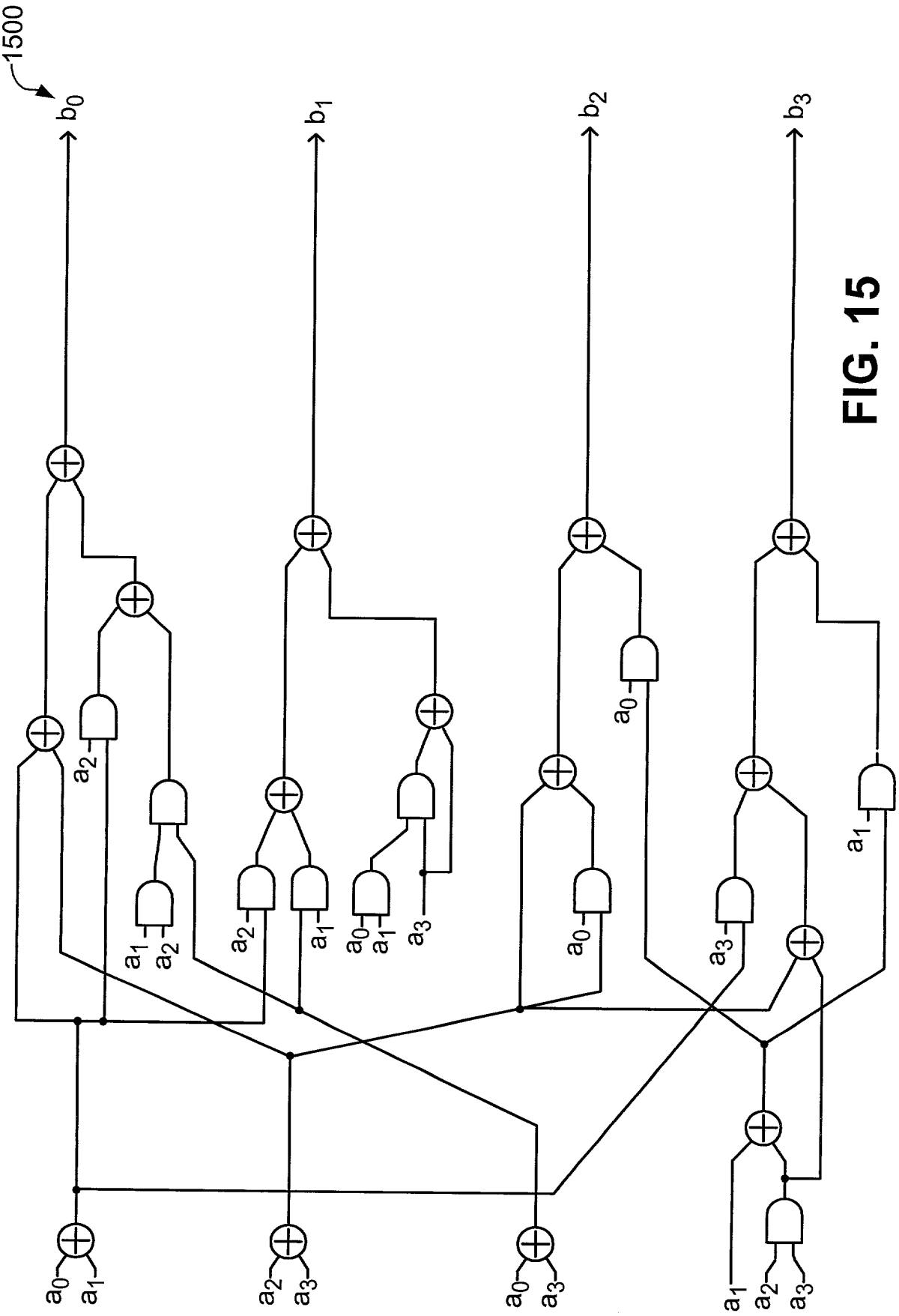


FIG. 15

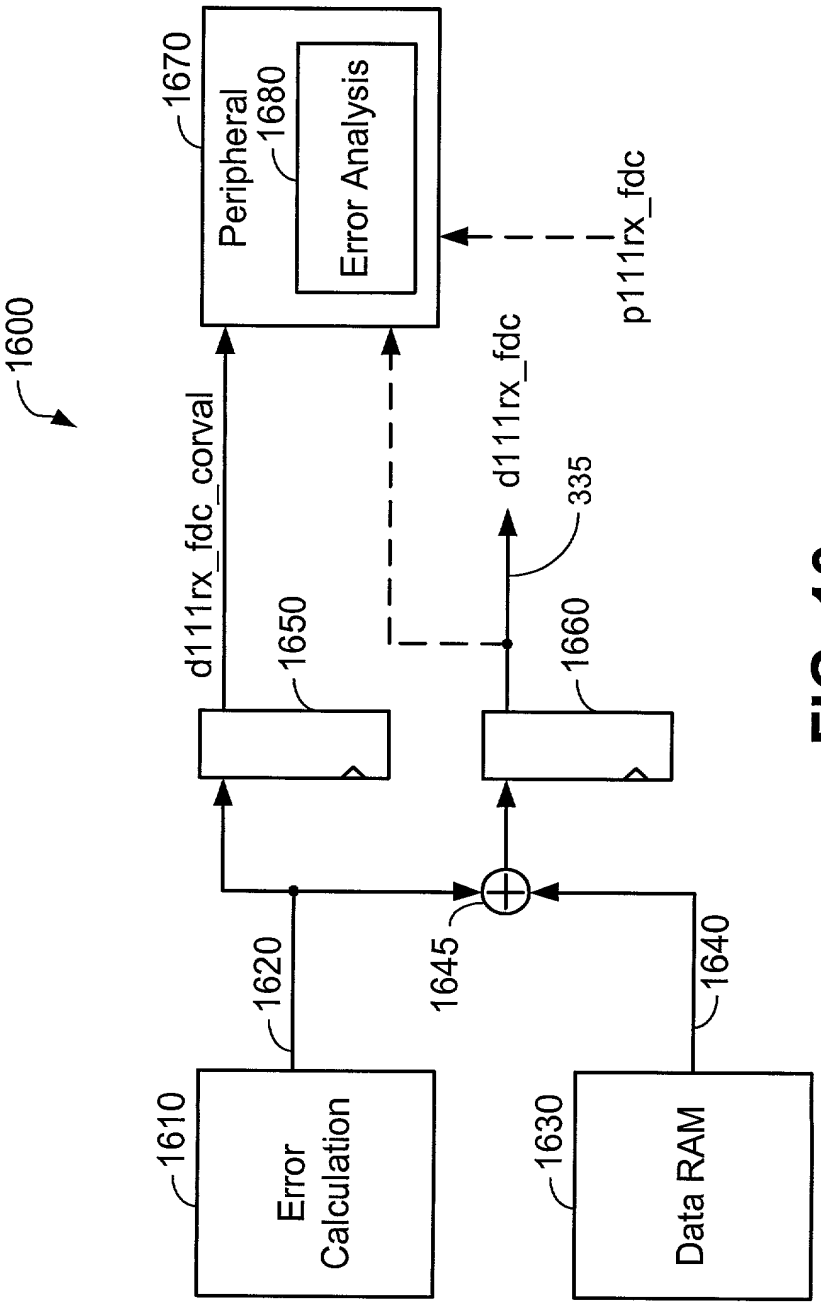

1600
1670
Peripheral
1680
Error Analysis
p111rx_fdc
d111rx_fdc_corval
d111rx_fdc
335
1650
1660
1620
1645
1640
1610
Error Calculation
1630
Data RAM

FIG. 16

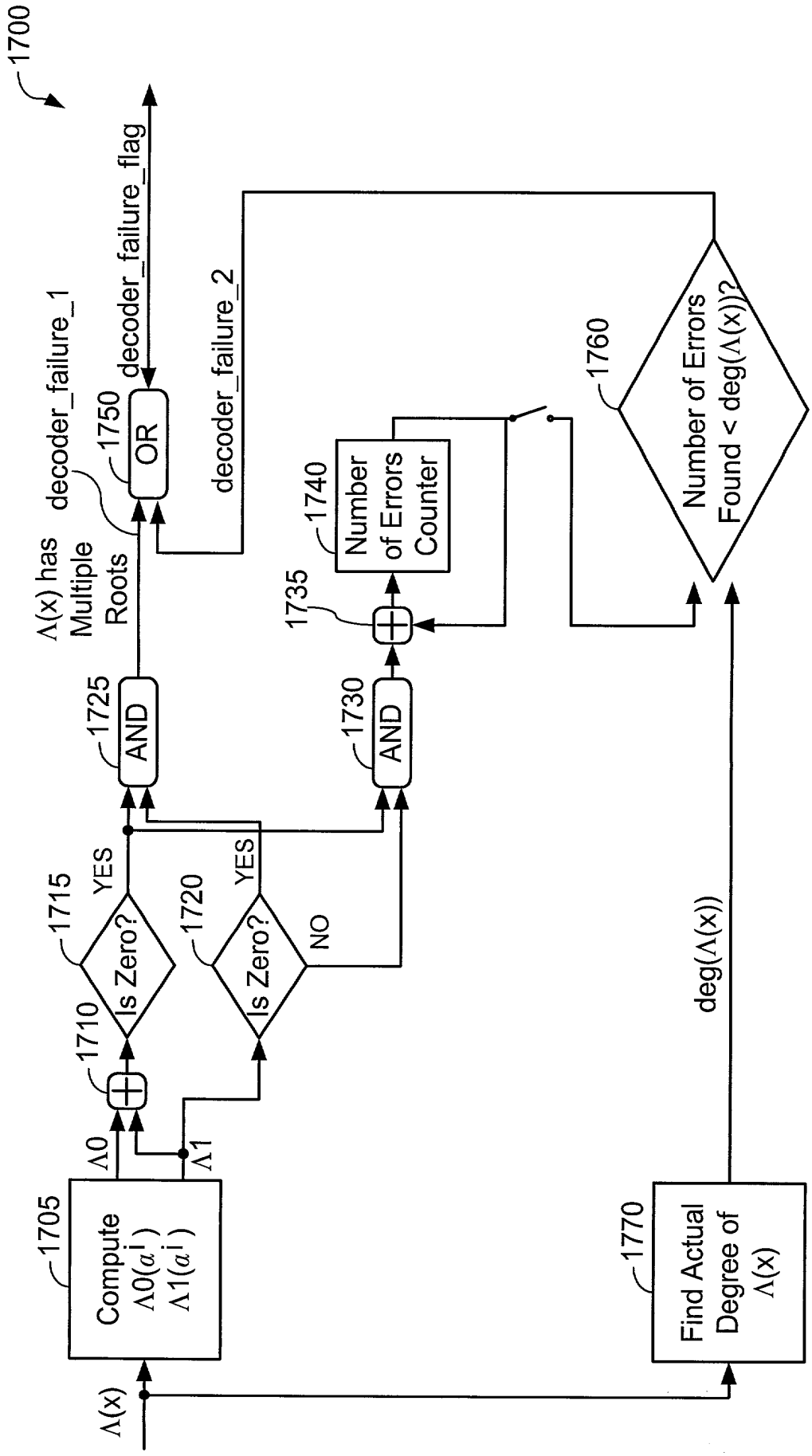

1700
decoder_failure_flag
decoder_failure_1
decoder_failure_2
1750
OR
Λ(x) has Multiple Roots
1725
AND
1730
AND
1735
1740
Number of Errors Counter
1760
Number of Errors Found < deg(Λ(x))?
1715
Is Zero?
YES
1720
Is Zero?
YES
NO
1710
Λ0
Λ1
1705
Compute Λ0(α^i) Λ1(α^i)
Λ(x)
deg(Λ(x))
1770
Find Actual Degree of Λ(x)

FIG. 17

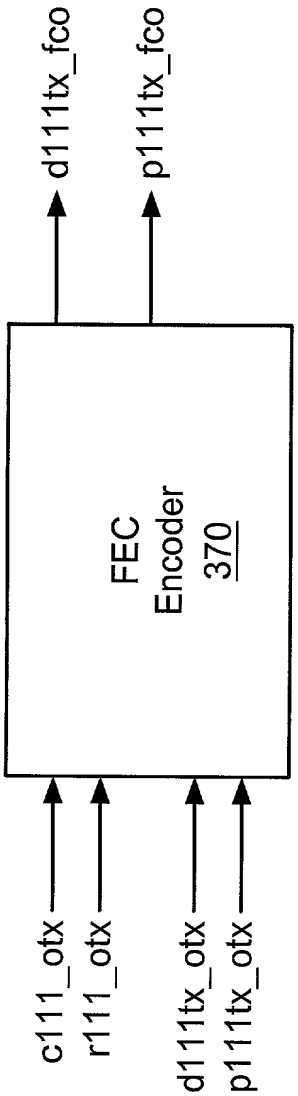

d111tx_fco
p111tx_fco
FEC
Encoder
370
c111_otx
r111_otx
d111tx_otx
p111tx_otx

FIG. 18

Name	Direction	Width	Description
c111_otx	IN	std_ulogic	System clock, 111 MHz
r111_otx	IN	std_ulogic	Signal for synchronous reset of encoder
d111tx_otx	IN	(383 down to 0)	Input data
p111tx_otx	IN	std_ulogic	Start of input FEC block pulse
d111tx_fco	BUFFER	(383 down to 0)	Output encoded data
p111tx_fco	BUFFER	std_ulogic	Pulse indicating the end of an FEC block

FIG. 19

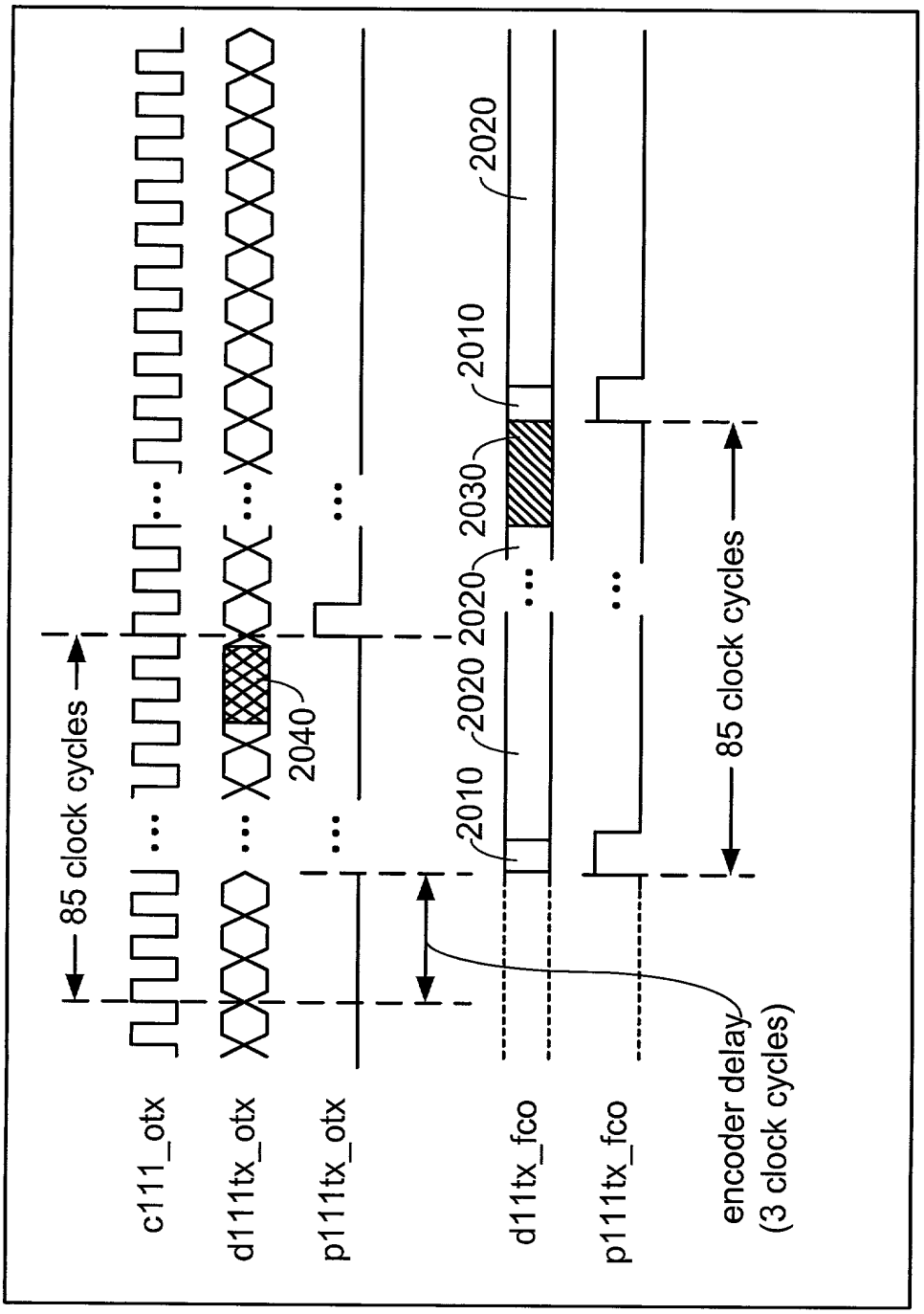
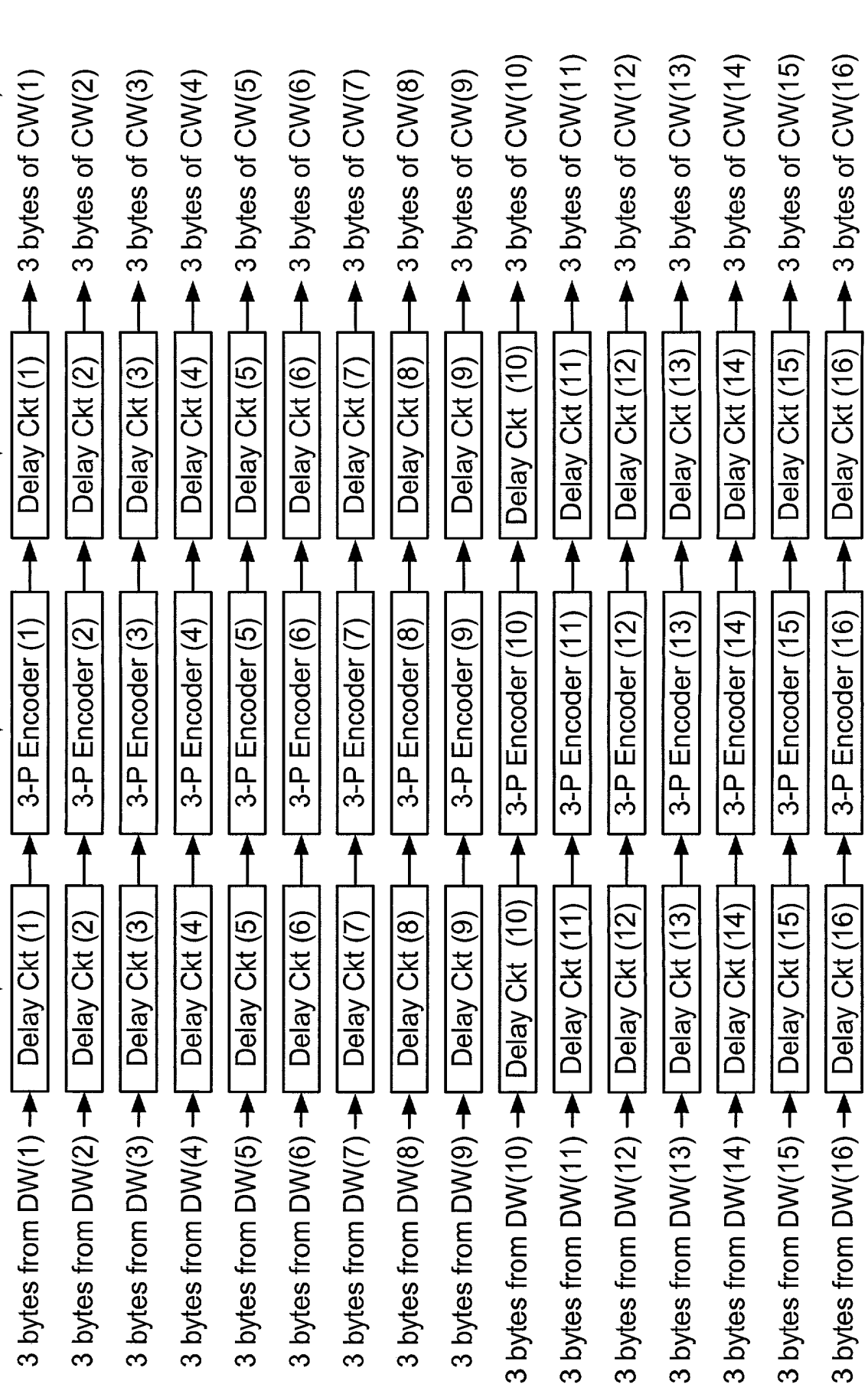

85 clock cycles
c111_otx
d111tx_otx
p111tx_otx
d11tx_fco
p111tx_fco
encoder delay
(3 clock cycles)
2040
2010
2020
2020
2030
2010
2020
85 clock cycles

FIG. 20

FIG. 21


370
2370
2200
2360
3 bytes from DW(1)
Delay Ckt (1)
3-P Encoder (1)
Delay Ckt (1)
3 bytes of CW(1)
3 bytes from DW(2)
Delay Ckt (2)
3-P Encoder (2)
Delay Ckt (2)
3 bytes of CW(2)
3 bytes from DW(3)
Delay Ckt (3)
3-P Encoder (3)
Delay Ckt (3)
3 bytes of CW(3)
3 bytes from DW(4)
Delay Ckt (4)
3-P Encoder (4)
Delay Ckt (4)
3 bytes of CW(4)
3 bytes from DW(5)
Delay Ckt (5)
3-P Encoder (5)
Delay Ckt (5)
3 bytes of CW(5)
3 bytes from DW(6)
Delay Ckt (6)
3-P Encoder (6)
Delay Ckt (6)
3 bytes of CW(6)
3 bytes from DW(7)
Delay Ckt (7)
3-P Encoder (7)
Delay Ckt (7)
3 bytes of CW(7)
3 bytes from DW(8)
Delay Ckt (8)
3-P Encoder (8)
Delay Ckt (8)
3 bytes of CW(8)
3 bytes from DW(9)
Delay Ckt (9)
3-P Encoder (9)
Delay Ckt (9)
3 bytes of CW(9)
3 bytes from DW(10)
Delay Ckt (10)
3-P Encoder (10)
Delay Ckt (10)
3 bytes of CW(10)
3 bytes from DW(11)
Delay Ckt (11)
3-P Encoder (11)
Delay Ckt (11)
3 bytes of CW(11)
3 bytes from DW(12)
Delay Ckt (12)
3-P Encoder (12)
Delay Ckt (12)
3 bytes of CW(12)
3 bytes from DW(13)
Delay Ckt (13)
3-P Encoder (13)
Delay Ckt (13)
3 bytes of CW(13)
3 bytes from DW(14)
Delay Ckt (14)
3-P Encoder (14)
Delay Ckt (14)
3 bytes of CW(14)
3 bytes from DW(15)
Delay Ckt (15)
3-P Encoder (15)
Delay Ckt (15)
3 bytes of CW(15)
3 bytes from DW(16)
Delay Ckt (16)
3-P Encoder (16)
Delay Ckt (16)
3 bytes of CW(16)

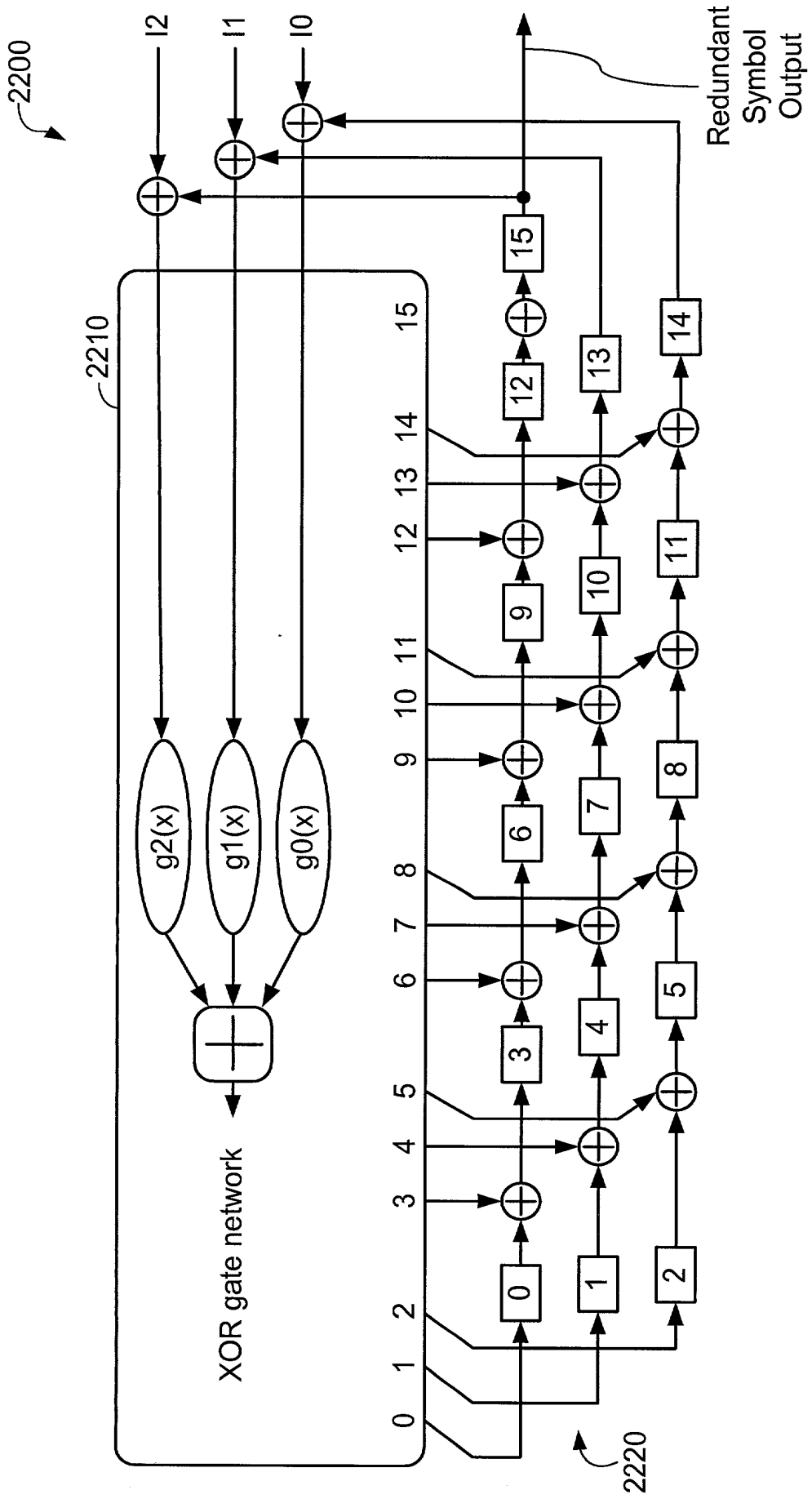

2200
I2
I1
I0
Redundant Symbol Output
2210
g2(x)
g1(x)
g0(x)
XOR gate network
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
2220

FIG. 22

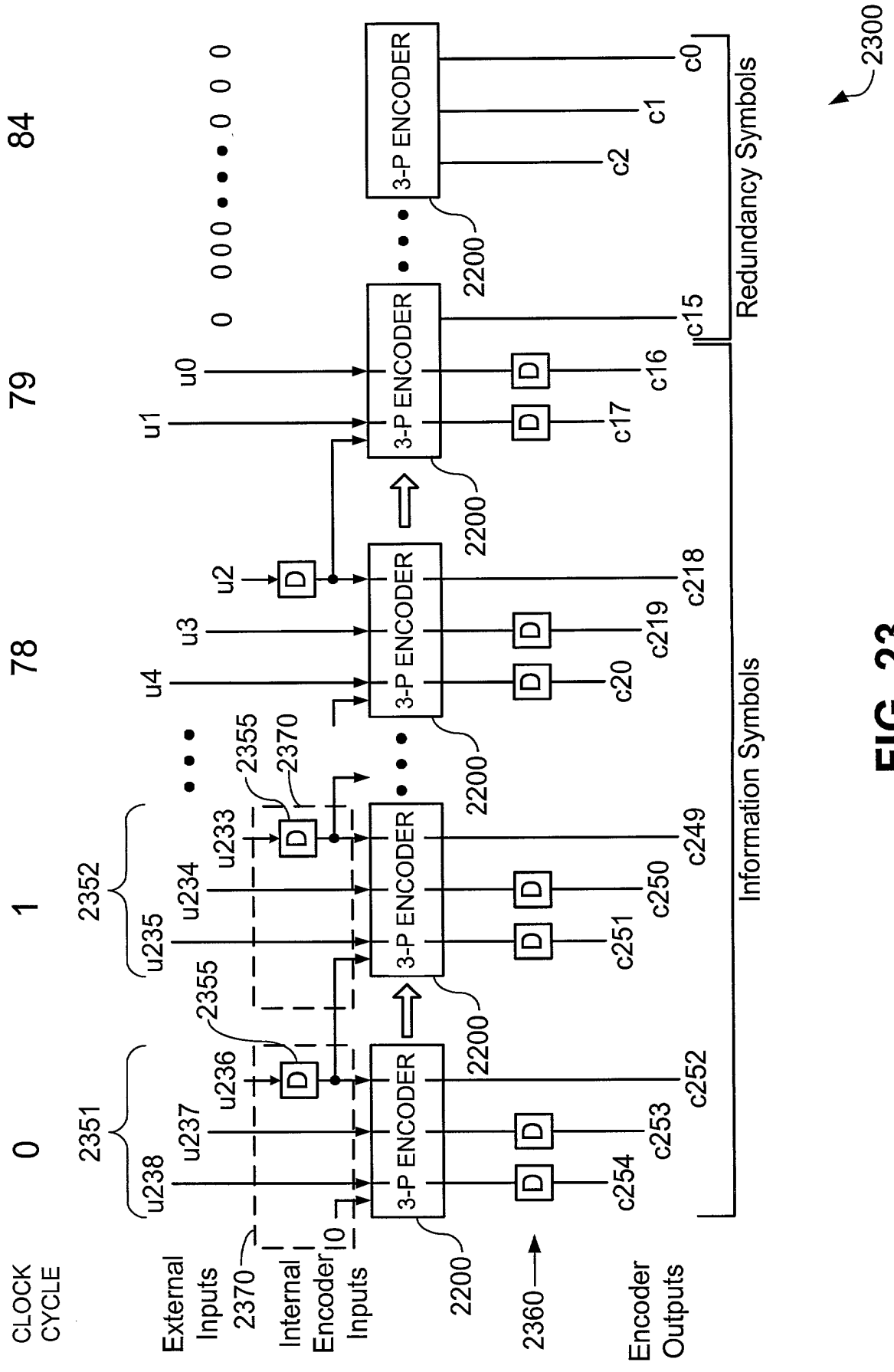

CLOCK CYCLE
0
1
78
79
84
External Inputs
2370
Internal Encoder Inputs
10
2351
2352
u238
u237
u236
u235
u234
u233
u4
u3
u2
u1
u0
0 0 0 0 • • • • 0 0 0 0
2355
2370
2200
3-P ENCODER
D
2360
Encoder Outputs
c254
c253
c252
c251
c250
c249
c220
c219
c218
c17
c16
c15
c2
c1
c0
Information Symbols
Redundancy Symbols
2300

FIG. 23